IN THE CLAIMS

A listing of all claims and their current status in accordance with 37 C.F.R. § 1.121(c) is provided below.

1. (currently amended) A computer system, comprising:

a first logic circuit;

a second logic circuit; and

an interface coupling the first logic circuit to the second logic circuit, wherein the interface includes:

an input logic block that receives an incoming data stream and a first clock from the first logic circuit, the input logic block provides an intermediate signal, wherein if the incoming data stream includes a first asserted signal, the intermediate signal inverts its logic state, wherein the input logic block includes;

a multiplexor, the multiplexor receives the incoming data stream; and

a first register coupled to the multiplexor; the first register is clocked by the first clock; wherein the multiplexor provides the first register the inverted version of the output of the first register when the incoming data stream includes the first asserted signal, the first register provides the intermediate signal.; and

an output logic block coupled to the input logic block, the output logic block receives the intermediate signal and a second clock, wherein the output logic block provides to the second logic circuit an output signal, the output signal is a second asserted

signal for one clock period of the second clock, when the output logic block detects a logic state change in the intermediate signal.

2. (original) The computer system of claim 1, wherein the first clock is not equal to the second clock.

3. (original) The computer system of claim 2, wherein the interface further includes a plurality of metastability registers coupled between the input logic block and the output logic block.

4. (cancelled)

5. (currently amended) The computer system of claim [[4]]1, wherein the output logic block includes,

a second register, the second register includes a second input and a second output, the second register is clocked by the second clock and receives the intermediate signal; and

an XOR gate coupled to the second register; wherein the second input and the second output of the second register is inputted to the XOR gate, the XOR gate provides the output signal.

6. (original) The computer system of claim 5, wherein the first logic circuit includes a plurality of Intel IA-64 microprocessors.

7. (original) The computer system of claim 5, wherein the second logic circuit is a plurality of PCI devices.

8. (original) The computer system of claim 7, wherein one of the plurality of PCI devices is a SCSI controller.

9. (original) The computer system of claim 5, wherein the second logic circuit does not receive the second asserted signal if the first logic circuit or the second logic circuit is reset.

10. (currently amended) An interface coupling a first logic circuit to a second logic circuit, comprising,

an input logic block that receives an incoming data stream and a first clock from the first logic circuit, the input logic block provides an intermediate signal, wherein if the incoming data stream includes a first asserted signal, the intermediate signal inverts its logic state, wherein the input logic block includes;

a multiplexor, the multiplexor receives the incoming data stream; and

a first register coupled to the multiplexor; the first register is clocked by the first clock; wherein the multiplexor provides the first register the inverted when the incoming data stream includes the first asserted signal, the first register provides the intermediate signal.;

and

an output logic block coupled to the input logic block, the output logic block receives the intermediate signal and a second clock, wherein the output logic block provides to the second logic circuit an output signal, the output signal is a second asserted

signal for one clock period of the second clock, when the output logic block detects a logic state change in the intermediate signal.

11. (original) The interface of claim 10, wherein the first clock does not equal the second clock.

12. (original) The interface of claim 11, wherein the interface further includes a plurality of metastability registers coupled between the input logic block and the output logic block.

13. (cancelled)

14. (currently amended) The interface of claim ~~13~~10, wherein the output logic block includes,

a second register, the second register includes a second input and a second output, the second register is clocked by the second clock and receives the intermediate signal; and

an XOR gate coupled to the second register; wherein the second input and the second output of the second register is inputted to the XOR gate, the XOR gate provides the output signal.

15. (original) The interface of claim 14, wherein the first logic circuit includes a plurality of Intel IA-64 microprocessors.

16. (original) The interface of claim 14, wherein the second logic circuit includes a plurality of PCI devices.

17. (original) The interface of claim 16, wherein the plurality of PCI devices includes a SCSI controller.

18. (original) The interface of claim 14, wherein the second logic circuit does not receive the second asserted signal if the first logic circuit or the second logic circuit is reset.

19. (original) A method for coupling a first logic circuit to a second logic circuit, comprising the step of:

providing an input data stream from a first logic circuit clocked by a first clock to a first register;

ascertaining a first asserted signal in the input data stream;

creating an intermediate signal by inverting the output of the first register when the first asserted signal is received;

comparing the logic states of the intermediate signal at different times, the different times equal to a first time period of a second clock;

outputting a second asserted signal to a second logic circuit for a period equaled to the second clock when the logic states of the intermediate signal are different during the first time period.

20. (original) The method of claim 19, wherein the first clock does not equal the second clock.

21. (original) The method of claim 20, further comprising the step of masking the second asserted signal if the first logic circuit or the second logic circuit receives a reset signal.

22. (original) The method of claim 20, wherein the first logic circuit is a plurality of Intel IA-64 microprocessors.

23. (original) The method of claim 20, wherein the second logic circuit is a plurality of PCI devices.

24. (original) The method of claim 23, wherein the plurality of PCI devices includes a SCSI controller.